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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/876,220	06/08/2001	Andrew B. Swaine	550-235	6509

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EXAMINER
BUEHL, BRETT J

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 02/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/876,220	SWAINE, ANDREW B.	
	Examiner	Art Unit	
	Brett J Buehl	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6/8/01,8/27/01,4/25/02,9/4/02,8/27/04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 April 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/4/02,8/27/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-21 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Declaration and Fees as received on 6/8/01, Oath as received on 8/27/01, Drawings as received on 4/25/02, IDS as received on 9/4/02, and IDS as received on 8/27/04.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

5. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

Claim Objections

6. Claims 1-14, 16 and 18-20 are objected to because of the following informalities:

a. Claim 1 recites the limitation, "Apparatus for processing data" in line 1 of each claim. This limitation should be amended to read as, "An apparatus for processing data", in order to more clearly define the processing apparatus being claimed.

b. Claims 2-14 recite the limitation, "Apparatus as claimed" in line 1 of each claim. This limitation should be amended to read as, "The apparatus as claimed", in order to be more grammatically correct.

c. Claim 16 recites the limitation, "A tracing tool as claimed" in line 1. This limitation should be amended to read as, "The tracing tool as claimed", in order to more clearly define the tracing tool being claimed.

d. Claims 18-20 recite the limitation, "A method as claimed" in line 1 of each claim. This limitation should be amended to read as, "The method as claimed", in order to more clearly define the method being claimed.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 2 and 19-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. Claim 2 recites the limitation "wherein for each instruction set the pattern of bits prepended to the specified instruction address bits of an instruction address from that instruction set is related by a shifted pattern with the pattern of bits prepended to the specified instruction address bits of instruction addresses of different instruction sets." This limitation is indefinite, as it is unclear to the examiner what is meant by a "shifted pattern" and how it relates the prepended patterns to one another. Revision of the claim language is necessary.

10. Claim 19 recites the limitation "the method of decompressing a compressed encoded instruction address" in line 1 of the claim. This limitation is indefinite, as it is unclear to the examiner if this claim is directed at the method of claim 18, which is a method of storing instruction set information, or a different method for decompressing the address.

11. Claim 21 recites the limitation "A computer program product carrying a computer program for controlling an apparatus in accordance with the method of claim 17." This limitation is indefinite, as it is unclear to the examiner if this claim was intended to be an independent claim, as claim 17 is a method claim and this limitation is directed toward a computer program product.

Claim Rejections – 35 USC § 101

12. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

13. Claims 17-21 rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The language of claims 17-20 is directed merely to an abstract idea that is not tied to a technological art, environment or machine which would result in a practical application producing a concrete, useful, and tangible result to form the basis of statutory subject matter under 35 U.S.C. 101.

The method steps are not directed to computer hardware and may be carried out through mental steps using only pencil and paper. Although the claim identifies a processing circuitry (i.e. computer hardware), there is no indication that hardware is necessary to carry out the method steps. For example, taking a first pattern of binary numbers (e.g. 0000000000000000), prepending a second pattern of binary numbers to the first pattern of binary numbers to indicate the instruction set to which the first pattern of binary numbers belongs (e.g. 010000000000000000), can be performed using only mental steps. This also includes the method steps of claims 18, 19 and 20, since partitioning the binary bits into subsections (e.g. 010 000 000 000 000 000), comparing them to a previous pattern (e.g. previous pattern = 010 000 000 000 001 100) of binary bits and outputting the subsections which differ from the previous pattern of binary bits (e.g. output only last two subsections since they were different = 001 100), can also be performed using only mental steps.

The examiner notes that in order to overcome the 35 USC 101 rejection for claim 21, the claim should be amended to read as "A computer readable medium carrying a computer program for controlling an apparatus in accordance with the method of claim 17."

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 1-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Advanced RISC Machines, "Embedded Trace Macrocell (Rev 0/0a): Specification", hereinafter ARM, and further in view of Nevill, GB 2307072 A.

16. Regarding claim 1, ARM has taught an apparatus for processing data, said apparatus comprising:

a. A processing circuit [ARM, Figure 1-1, Page 1-3] for executing processing instructions from any of a plurality of instruction sets of processing instructions [ARM and Thumb, Section 1.1.1, Page 1-4], each processing instruction being specified by an instruction address identifying that processing instruction's location in memory [It is inherent that instructions have an associated address in memory], a different number of instruction address bits needing to be specified in the instruction address for processing instructions in different instruction sets [Section 2.5.1, Page 2-8, 5th paragraph, bit 1 of the address for ARM instructions is ignored, therefore, more bits are required for the Thumb instructions than the ARM instructions]; and

b. Encoding logic for encoding an instruction address with an indication of the instruction set corresponding to that instruction to generate an n-bit encoded instruction

address [Section 2.5.1, Page 2-8, 4th paragraph, the logic that encoded bit 0 of the instruction address is inherent], the encoding logic being arranged to perform the encoding by performing a computation equivalent to extending the specified instruction address bits to n-bits by prepending a bit to the specified instruction address bits, the bit prepended being dependent on the instruction set corresponding to that instruction [The indication is prepended to the instruction address with the indication depending of the instruction set type of the corresponding instruction (LOW for ARM, HIGH for Thumb)].

ARM has not explicitly taught prepending a pattern of bits (i.e. more than one bit) to the specified instruction address bits, as only one bit is required to differentiate between the two instruction sets taught.

17. However, Nevill has taught a data processing apparatus for processing a plurality of instruction sets, stating "it is known to provide systems that execute program instruction words from two or more instruction sets, with means being provided to switch between use of the different instruction sets" [Page 1, lines 11-13]. This is accomplished by "defining a predetermined bit or bits of the program counter register (PC) to indicate the instruction set to be used" [Page 3, lines 27-29], meaning more than one bit is required when three or more instruction sets are supported. One of ordinary skill in the art would have recognized that prepending a pattern of bits (i.e. more than one), instead of only one bit, to the instruction addresses in ARM would allow the apparatus to function with processors supporting more than two instruction sets, thereby allowing each and every instruction set supported by the processor to be uniquely identified by the apparatus of ARM. Expanding the capabilities of the ARM apparatus was suggested in ARM, which stated "[bit 1 of the address for ARM instruction

accesses] is reserved for future expansion" [ARM, Section 2.5.1, 5th paragraph]. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have modified the apparatus of ARM to expand the number of instruction sets uniquely identifiable by the apparatus by prepending a pattern of bits (i.e. more than one) to the instruction addresseses.

18. Regarding claim 2, ARM, in view of Nevill, has taught the apparatus as claimed in claim 1, wherein for each instruction set the pattern of bits prepended to the specified instruction address bits of an instruction address from that instruction set is related by a shifted pattern with the pattern of bits prepended to the specified instruction address bits of instruction addresses of different instruction sets [Prepending two bits to instruction addresses, which represents three instructions sets, yields '00', '01' and '10' as the prepended patterns. A pattern '0010', when shifted through a two-bit window (making it a shifted pattern), relates the three prepended patterns to one another, in that shifting the pattern through a two-bit window yields the three prepended patterns (i.e. 0010, 0010 and 0010).].

19. Regarding claim 3, ARM, in view of Nevill, has taught the apparatus as claimed in claim 1, wherein the encoding logic is arranged to perform the encoding by performing a computation equivalent to generating an intermediate value by pre-pending a predetermined pattern of bits to the specified instruction address bits of the instruction address and then selecting as the encoded instruction address n bits from the intermediate value [Section 2.5.1, Page 2-8, 4th paragraph, the indication is prepended to the instruction address, creating an intermediate value, then all bits are selected from the intermediate value].

20. Regarding claim 4, ARM, in view of Nevill, has taught the apparatus as claimed in claim 1, further comprising compression logic for compressing a said encoded instruction address by

performing a computation equivalent to partitioning that encoded instruction address into a plurality of x-bit sections, comparing each x-bit section with the corresponding x-bit section of a preceding encoded instruction address and outputting as a compressed encoded instruction address the most significant x-bit section that differs from the corresponding x-bit section of the preceding encoded instruction address, along with any less significant x-bit sections [Section 2.5.1, Compressed branch address packet structure, page 2-9, 4th paragraph].

21. Regarding claim 5, ARM, in view of Nevill, has taught the apparatus as claimed in claim 4, wherein the compression logic is arranged to associate with each x-bit section to be output from the compression logic a flag to indicate whether that x-bit section is the last x-bit section being output as the compressed encoded instruction address [Section 2.5.1, Compressed branch address packet structure, page 2-9, 3rd paragraph].

22. Regarding claim 6, ARM, in view of Nevill, has taught the apparatus as claimed in claim 5, wherein if a plurality of x-bit sections are to be output from the compression logic, the plurality of x-bit sections are output sequentially starting with the least significant x-bit section [Section 2.5.1, Compressed branch address packet structure, page 2-10, the flag bit indicates if there are additional packets in the address stream, the most significant packet has an indication that there are no more packets, meaning the least significant packets are sent first].

23. Regarding claim 7, ARM, in view of Nevill, has taught the apparatus as claimed in claim 5, wherein the compression logic is further arranged to expand to y bits each x-bit section to be output from the compression logic, with the most significant y-x bits containing the flag [Section 2.5.1, Compressed branch address packet structure, page 2-9, the flag bit is appended to the address packets as bit 7 (MSB), making the packets 8-bits in length].

24. Regarding claim 8, ARM, in view of Nevill, has taught the apparatus as claimed in claim 7, wherein the flag is a single bit [Section 2.5.1, Compressed branch address packet structure, page 2-9].

25. Regarding claim 9, ARM, in view of Nevill, has taught the apparatus as claimed in claim 8, wherein y is 8 and x is 7 [Section 2.5.1, Compressed branch address packet structure, page 2-9, the compressed packet length is 8 bits, including the flag bit, therefore, the encoded packet length was 7 bits before the flag bit was appended to the compressed packet to make it 8 bits].

26. Regarding claim 10, ARM, in view of Nevill, has taught the apparatus as claimed in claim 1, but has not explicitly taught wherein the encoding logic comprises an n-bit selector logic unit for receiving the intermediate value and an identifier signal identifying the instruction set associated with the instruction address contained within the intermediate value, the n-bit selector being arranged to output a predetermined n-bits of the intermediate value dependent on the identifier signal.

27. However, Nevill states that "the program counter register is a 32-bit register, which allows 2^32 bytes to be addressed in the memory system…since this equates to 4 gigabytes of addressable memory space, it is extremely unlikely that the full address range made possible…will be required" [Page 7, lines 11-15]. Furthermore, the apparatus of ARM attempts to limit the amount of data saved and sent for tracing. Providing a selector circuit in the encoding logic that only selects a subset of bits from the intermediate signal would allow the instruction address to be compressed even further. Therefore, it would have been obvious to one of ordinary skill in the art to have modified the apparatus of ARM, in view of Nevill, to include a

selector circuit in the encoder logic in order to allow for only a subset of bits to be sent to the compression logic.

28. Regarding claim 11, ARM, in view of Nevill, has taught the apparatus as claimed in claim 4, wherein the compression logic comprises a plurality of comparators, each comparator being arranged to receive a corresponding x-bit section of the encoded instruction address, and including temporary storage for storing the corresponding x-bit section of the preceding encoded instruction address, the comparator being arranged to compare the two x-bit sections and to generate a difference signal which is set when the two x-bit sections are different [Section 2.5.1, Compressed branch address packet structure, page 2-9. The compression logic "registers the last branch address that it has broadcast" and compares the preceding branch address to the current address in sections, therefore, it is inherent that there are a plurality of comparators to compare the individual sections. It is inherent that a difference signal be present in order to indicate that the flag bit should or should not be set.].

29. Regarding claim 12, ARM, in view of Nevill, has taught the apparatus as claimed in claim 11, wherein the compression logic further comprises a flag generator logic arranged to generate for each x-bit section to be output from the compression logic a flag based on predetermined combinations of the difference signals generated by the plurality of comparators, such that a flag for a particular x-bit section is set if a more significant x-bit section is also to be output [Section 2.5.1, Compressed branch address packet structure, page 2-9. The packets are sent in sequential order with the least significant packet being first. The flag is only set if there are additional packets in the address stream. Therefore, it is inherent that there is flag generator logic to set the flag according to different combinations of the difference signals.].

30. Regarding claim 13, ARM, in view of Nevill, has taught the apparatus as claimed in claim 12, wherein the compression logic further comprises an output generator for generating the compressed encoded instruction address by pre-pending to each x-bit section to be output its corresponding flag, thereby generating as the output compressed encoded instruction address a sequence of y-bit sections [Section 2.5.1, Compressed branch address packet structure, page 2-9. It is inherent that there is an output generator logic to prepend the flag bit to the address packets.].

31. Regarding claim 14, ARM, in view of Nevill, has taught the apparatus as claimed in claim 4, wherein the encoding logic and compression logic are provided within a trace module used to trace activities of the processing circuit [Section 2.2, Structure of the trace port, page 2-3, the device is an Embedded Trace Macrocell used for tracing the activities of the processor].

32. Regarding claim 15, given the similarities between the claims, the arguments as stated for claim 1 are also applicable to claim 15.

33. Regarding claim 16, given the similarities between the claims, the arguments as stated for claim 4 are also applicable to claim 16.

34. Regarding claim 17, given the similarities between the claims, the arguments as stated for claims 1 and 2 are also applicable to claim 17.

35. Regarding claim 18, given the similarities between the claims, the arguments as stated for claim 4 are also applicable to claim 18.

36. Regarding claim 19, ARM, in view of Nevill, has taught the method according to claim 18, but is silent on the method further comprising the steps of decompressing the compressed, encoded instruction address.

37. However, examiner takes OFFICIAL NOTICE that decompressing the compressed, encoded instruction address would be accomplished by reversing the process of compression. The compression method determines the packets that are different from the previous instruction address, sets the appropriate flag bits and sends only the difference packets. Reversing the process would comprise the steps of determining the number of packets sent (using the flag bits), and replacing the missing packets (the total number of packets should be five) with the corresponding packets of the previous instruction address. Therefore, it would have been obvious to one of ordinary skill in the art to have modified the method ARM, in view of Nevill, to further comprise the steps decompressing the compressed, encoded instruction address by reversing the process of compression.

38. Regarding claim 20, ARM, in view of Nevill, has taught the method as claimed in claim 19, but is silent on the method further comprising the step of decoding the encoded instruction address by performing a computation equivalent to determining from the predetermined pattern of bits the instruction set to which the instruction address relates, and removing the predetermined pattern of bits to yield the specified instruction address bits.

39. However, the examiner takes OFFICIAL NOTICE that decoding the encoded instruction address would be accomplished by removing the prepended instruction set indication bits, yielding the instruction address. Therefore, it would have been obvious to one of ordinary skill in the art to have modified the method of ARM, in view of Nevill, to further comprise the steps of decoding the encoded instruction address by reversing the process of encoding.

40. Regarding claim 21, ARM, in view of Nevill, has taught a computer program product carrying a computer program for controlling an apparatus in accordance with the method of

claim 17 [It is inherent that there is a computer program for controlling an apparatus in accordance with the method claim 17, which must be contained on a computer program product for it to be statutory.].

Conclusion

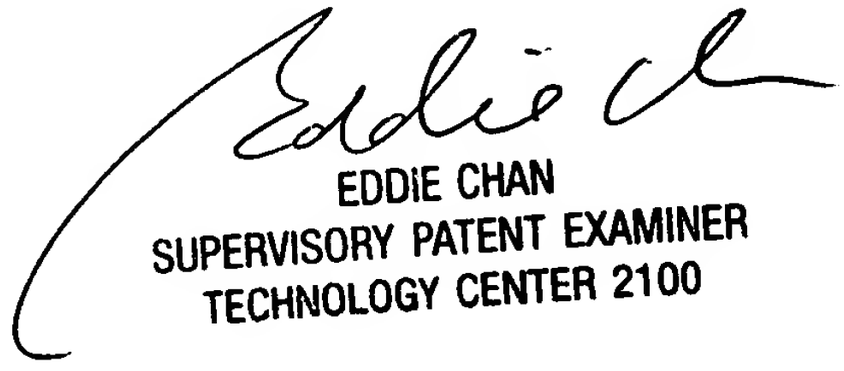
41. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of art disclosed by the references cited and the objections made. Applicant must show how the amendments avoid such references and objections. See 37 CFR 1.111(c).

42. Inquiries concerning this communication or earlier communications from the examiner should be directed to Brett J. Buehl who can be reached at (571) 272-4161 or <brett.buehl@uspto.gov>. The examiner's normal working schedule is between the hours 9:00am – 6:30pm (EST), Monday – Friday, with alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan, can be reached at (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

43. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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